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(54) **SYSTEM FOR A WIDE TEMPERATURE RANGE NONVOLATILE MEMORY**

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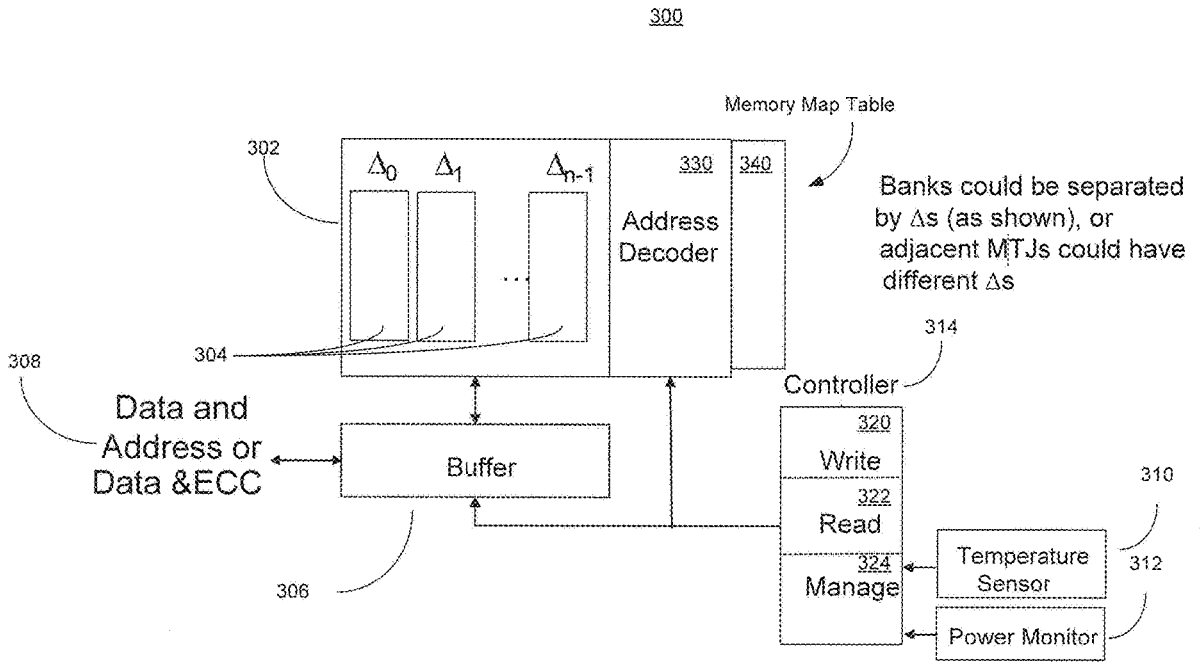
(57) **ABSTRACT**

A system for a nonvolatile memory for broad temperature range applications. The system includes a memory organized into an addressable memory range and comprising a plurality of memory arrays comprising memory cells wherein each memory array is configured for operation over a different temperature range, and a buffer for receiving a data word and an associated address for writing into the memory. A temperature sensor is used for sensing a current temperature of operation of the memory. A write controller is coupled to the buffer, the temperature sensor and the memory. The write controller is operable to perform a write operation that includes accessing a temperature value from the temperature sensor, selecting a selected memory array of the plurality of memory arrays that is configured for operation at the temperature value, and writing the data word, at the associated address, to the selected memory array.



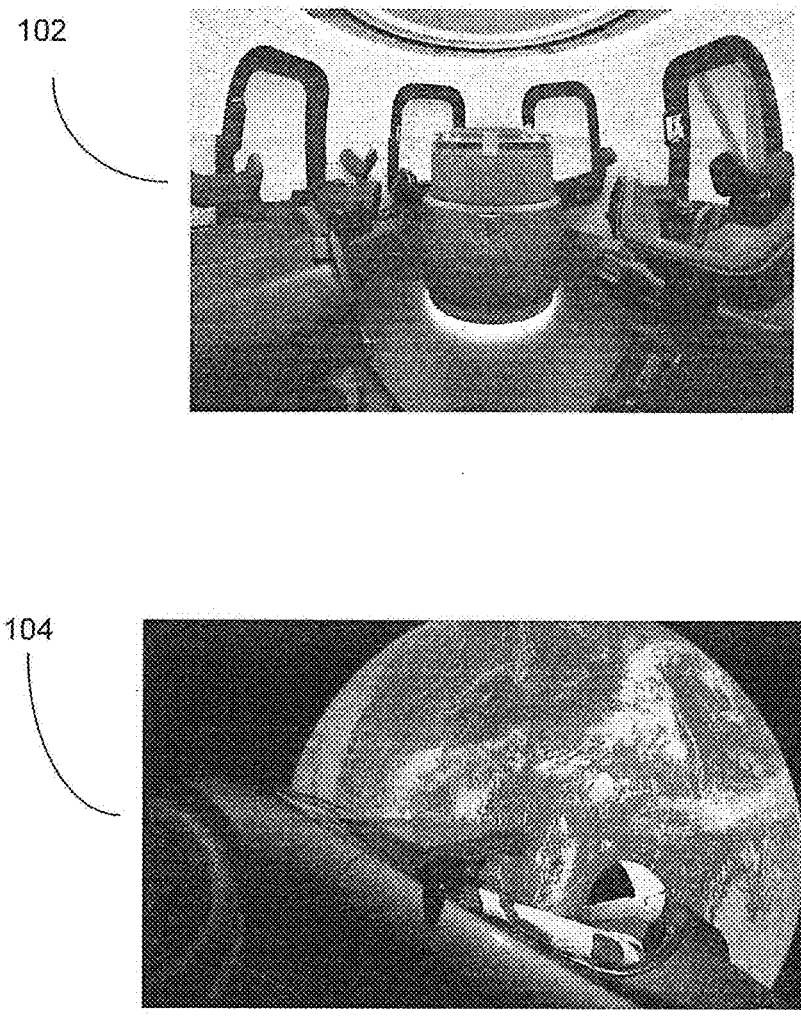


FIG. 1

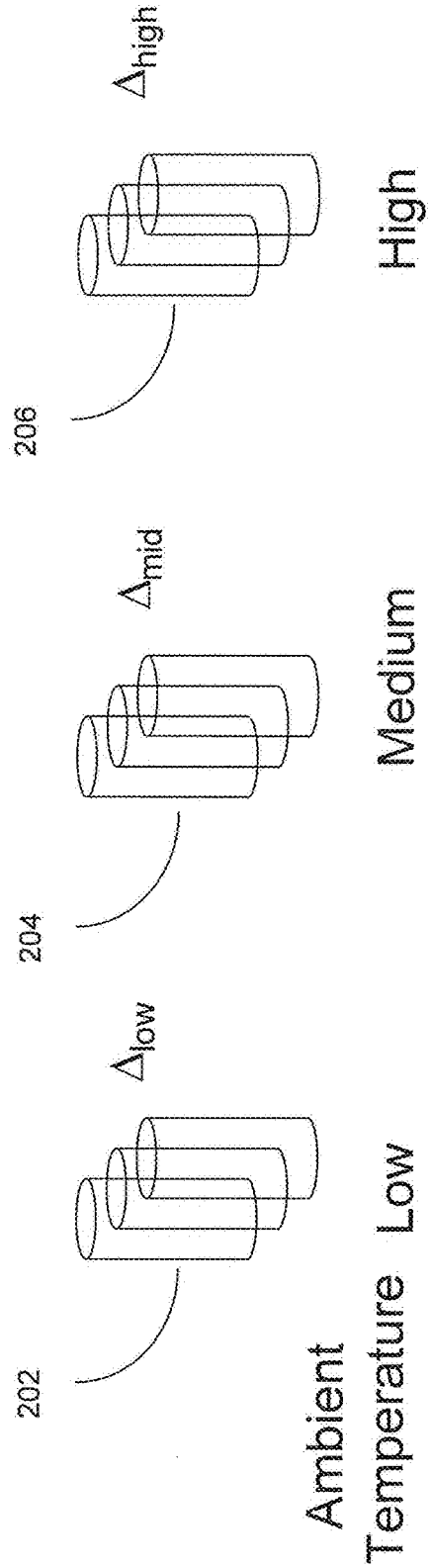

Ambient Temperature
Low
Medium
High
202
204
206
Δ_{low}
Δ_{mid}
Δ_{high}

FIG. 2

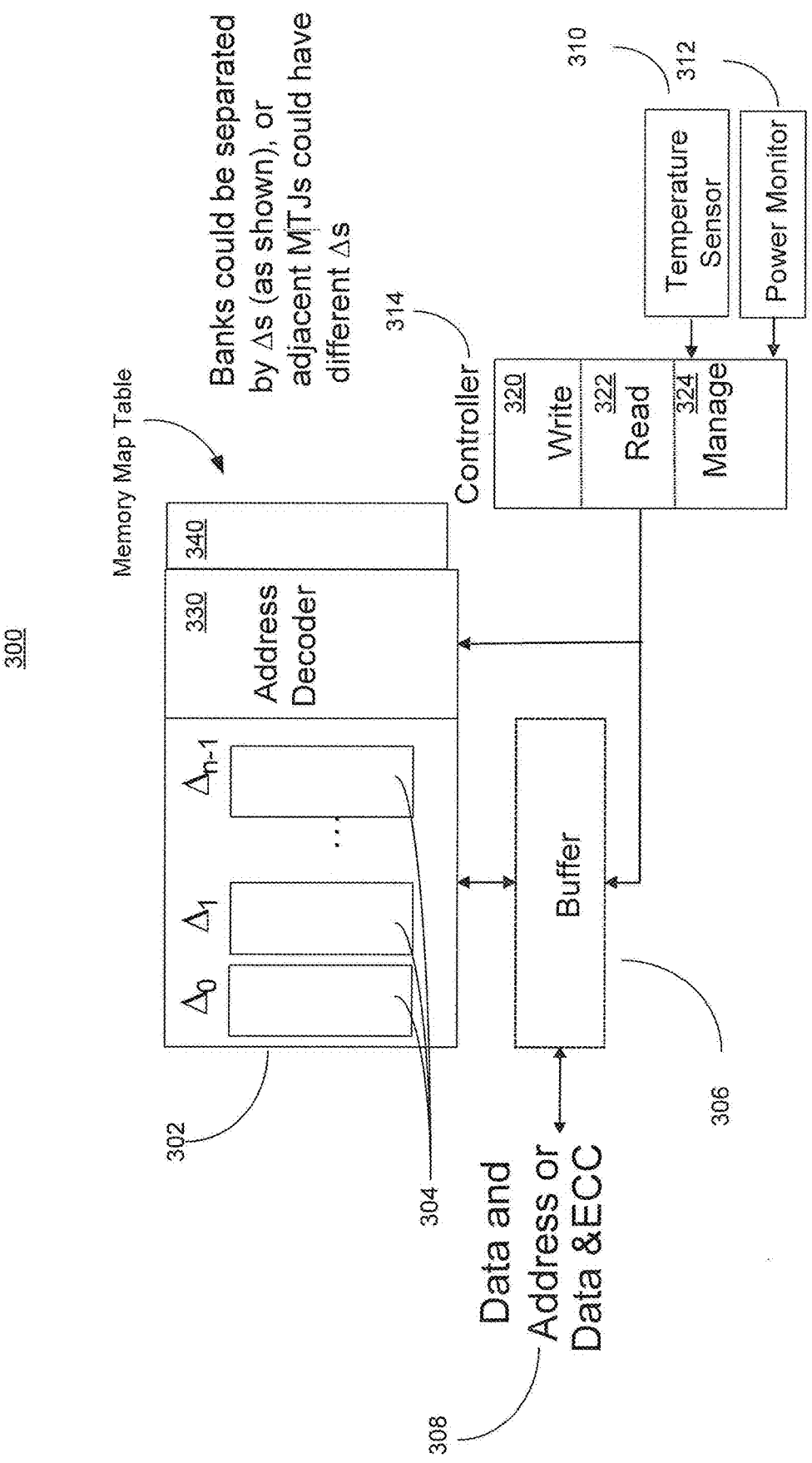

300
Memory Map Table
Banks could be separated by Δs (as shown), or adjacent MTJs could have different Δs
314
Controller
320
Write
322
Read
324
Manage
310
Temperature Sensor
312
Power Monitor
340
330
Address Decoder
Δ_{n-1}
Δ_1
Δ_0
Buffer
302
304
306
308
Data and Address or Data &ECC

FIG. 3

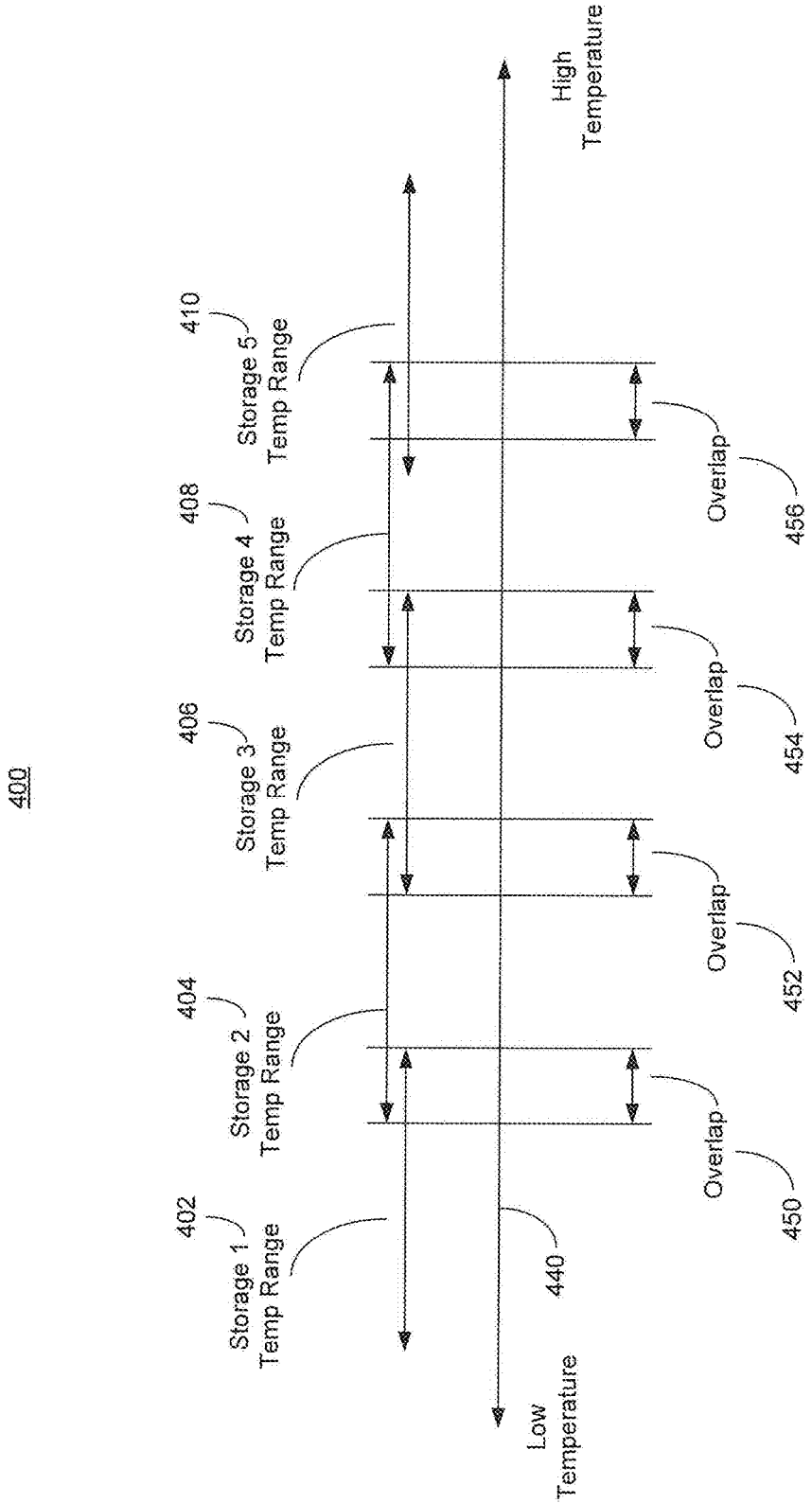

400
High Temperature
Low Temperature
440
402
Storage 1 Temp Range
404
Storage 2 Temp Range
406
Storage 3 Temp Range
408
Storage 4 Temp Range
410
Storage 5 Temp Range
450
Overlap
452
Overlap
454
Overlap
456
Overlap

FIG. 4

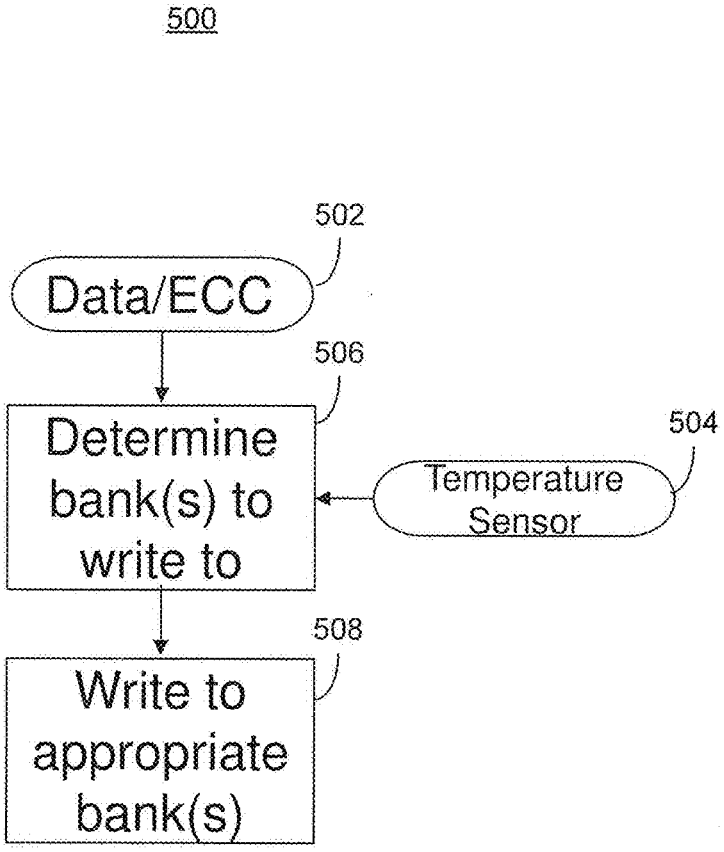

500
502
Data/ECC
506
Determine bank(s) to write to
504
Temperature Sensor
508
Write to appropriate bank(s)

FIG. 5A

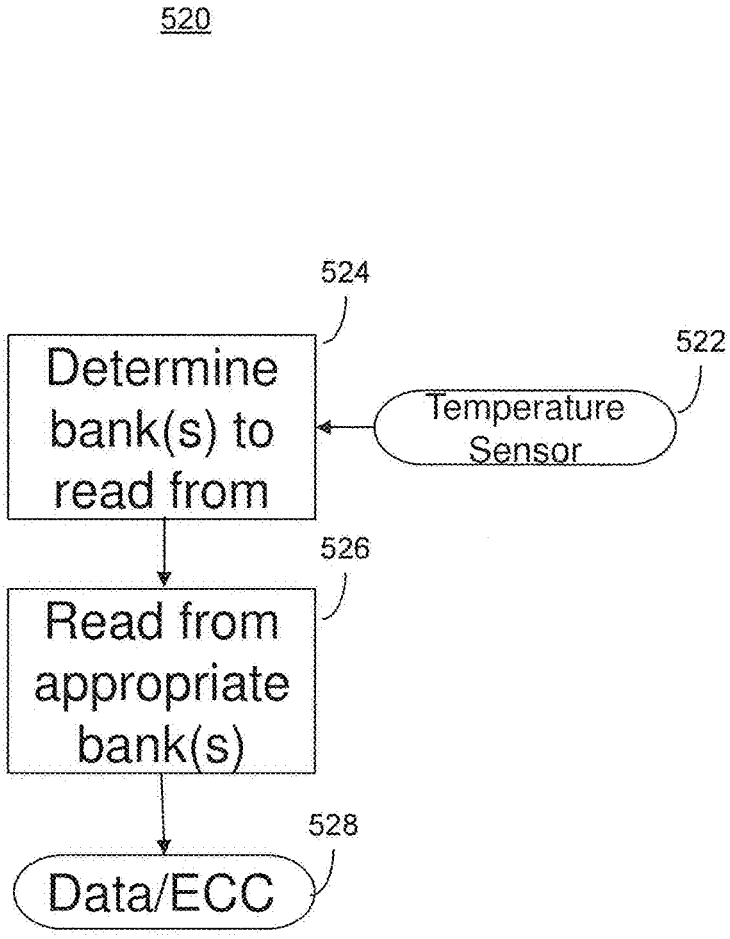

520
524
Determine bank(s) to read from
522
Temperature Sensor
526
Read from appropriate bank(s)
528
Data/ECC

FIG 5B

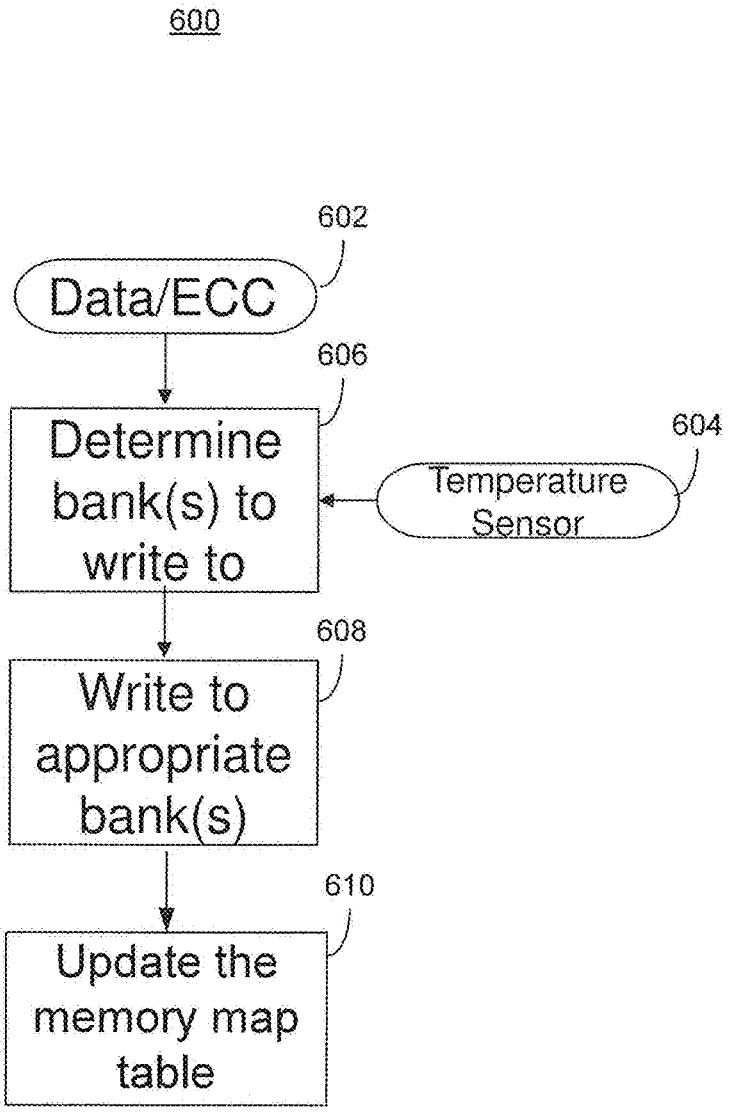

600
602
Data/ECC
606
Determine bank(s) to write to
604
Temperature Sensor
608
Write to appropriate bank(s)
610
Update the memory map table

FIG 6A

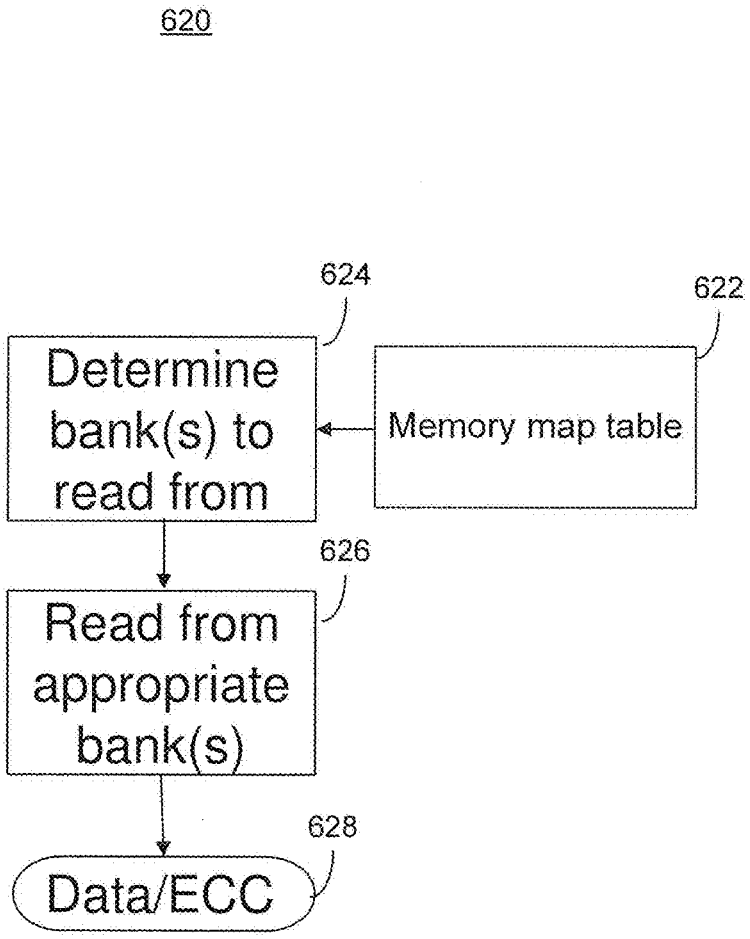

620
624
622
Determine bank(s) to read from
Memory map table
626
Read from appropriate bank(s)
628
Data/ECC

FIG 6B

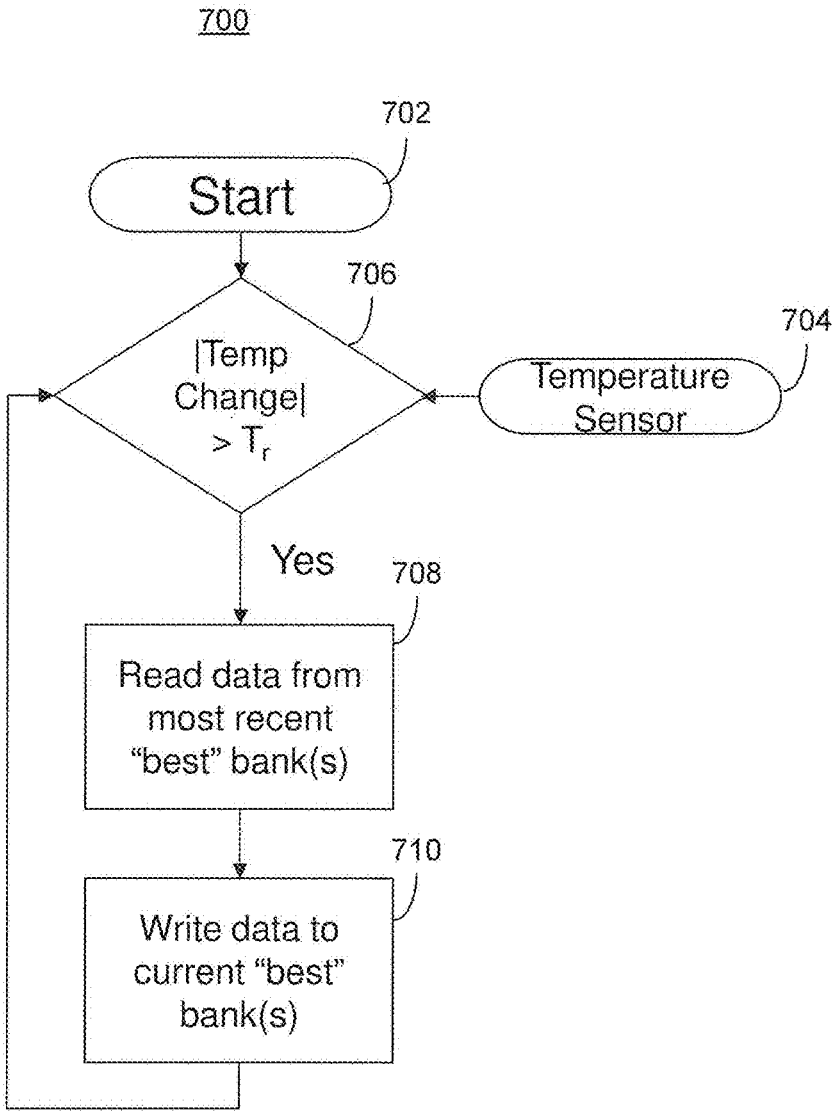

700
702
Start
706
|Temp Change| > T_r
704
Temperature Sensor
Yes
708
Read data from most recent "best" bank(s)
710
Write data to current "best" bank(s)

FIG 7

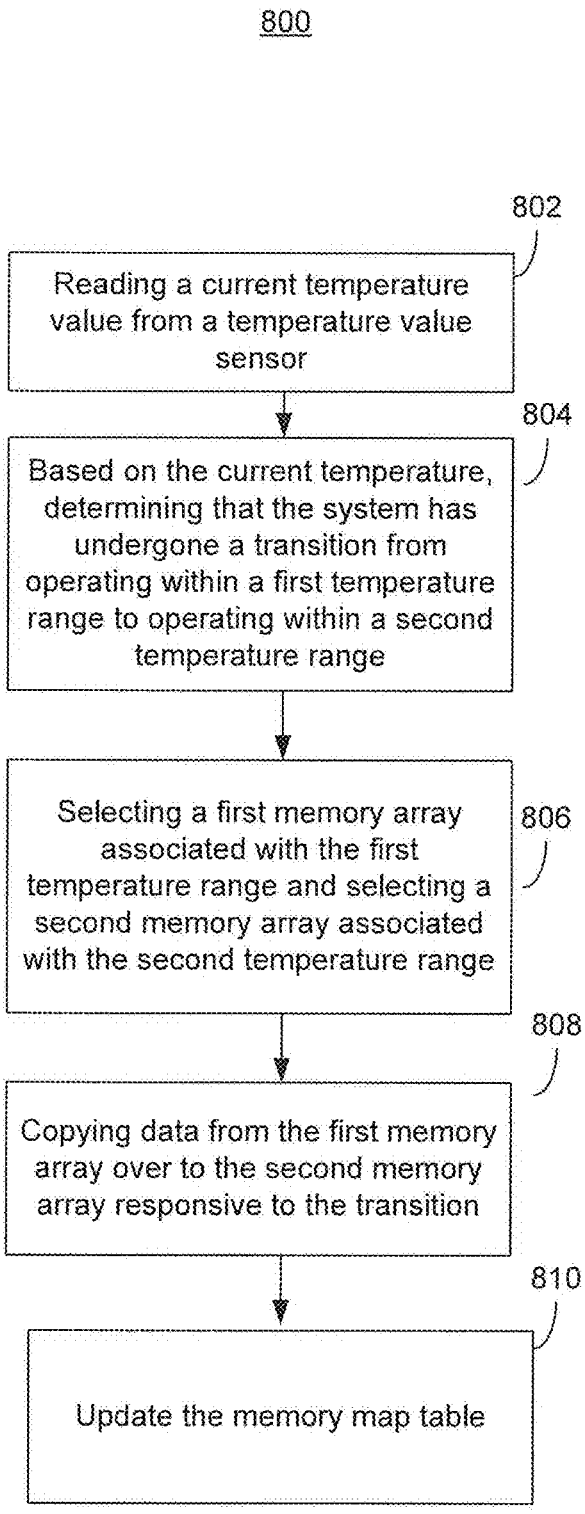

800
802
Reading a current temperature value from a temperature value sensor
804
Based on the current temperature, determining that the system has undergone a transition from operating within a first temperature range to operating within a second temperature range
806
Selecting a first memory array associated with the first temperature range and selecting a second memory array associated with the second temperature range
808
Copying data from the first memory array over to the second memory array responsive to the transition
810
Update the memory map table

FIG 8

SYSTEM FOR A WIDE TEMPERATURE RANGE NONVOLATILE MEMORY

FIELD OF THE INVENTION

[0001] Embodiments of the present invention are generally related to integrated circuit structures used in memory systems that can be used by computer systems, including embedded computer systems.

BACKGROUND OF THE INVENTION

[0002] Magnetoresistive random-access memory ("MRAM") is a non-volatile memory technology that stores data through magnetic storage elements. These elements are two ferromagnetic plates or electrodes that can hold a magnetic field and are separated by a non-magnetic material, such as a non-magnetic metal or insulator. This structure is known as a magnetic tunnel junction (MTJ).

[0003] MRAM devices can store information by changing the orientation of the magnetization of the free layer of the MTJ. In particular, based on whether the free layer is in a parallel or anti-parallel alignment relative to the reference layer, either a one or a zero can be stored in each MRAM cell. Due to the spin-polarized electron tunneling effect, the electrical resistance of the cell changes due to the orientation of the magnetic fields of the two layers. The electrical resistance is typically referred to as tunnel magnetoresistance (TMR) which is a magnetoresistive effect that occurs in a MTJ. The cell's resistance will be different for the parallel and anti-parallel states and thus the cell's resistance can be used to distinguish between a one and a zero. One important feature of MRAM devices is that they are non-volatile memory devices, since they maintain the information even when the power is off.

[0004] MRAM devices are considered as the next generation structures for a wide range of memory applications. MRAM products based on spin transfer torque transfer switching are already making its way into large data storage devices. Spin transfer torque magnetic random access memory (STT-MRAM), or spin transfer switching, uses spin-aligned (polarized) electrons to change the magnetization orientation of the free layer in the magnetic tunnel junction. In general, electrons possess a spin, a quantized number of angular momentum intrinsic to the electron. An electrical current is generally unpolarized, e.g., it consists of 50% spin up and 50% spin down electrons. Passing a current though a magnetic layer polarizes electrons with the spin orientation corresponding to the magnetization direction of the magnetic layer (e.g., polarizer), thus produces a spin-polarized current. If a spin-polarized current is passed to the magnetic region of a free layer in the MTJ device, the electrons will transfer a portion of their spin-angular momentum to the magnetization layer to produce a torque on the magnetization of the free layer. Thus, this spin transfer torque can switch the magnetization of the free layer, which, in effect, writes either a one or a zero based on whether the free layer is in the parallel or anti-parallel states relative to the reference layer.

[0005] The fabrication of MRAM involves the formation of small MTJ (Magnetic Tunnel Junction) patterns in pillar shapes. The pillars or pillar structures can be patterned on a hard mask layer and then transferred to MTJ films. The patterning of pillars on a hard mask layer is traditionally done using an electron beam lithography in a research environment. However, for high volume production, electron beam patterning is not cost effective as the process is very slow. Alternately, these pillars can be patterned using optical lithography tools. Optical lithography resolution is limited by diffraction. Since the pillars, when printed onto a layer of photoresist, are two dimensional features, it is more challenging to achieve the same resolution as the resolution can be achieved by a-1D pattern such as a line.

[0006] Importantly, it is known that by altering the semiconductor fabrication process for MTJ MRAM cells, the optimum temperature range over which the cells operate can be adjusted. Depending upon the particular fabrication process, memory cells can be fabricated with a different A to operate at different temperatures (e.g., low temperature, medium temperature, high temperature, etc.).

[0007] The nonvolatile aspect of MRAM makes its use in certain applications extremely valuable. For example, automotive, aerospace, and military uses require broad temperature range operability, and space tourism, heavy manufacturing in space, colonization and mining of moons, asteroids, and planets are all under serious research and development by many companies around the world. Reliable data and reliable datacenters will likely be necessary for both manned and unmanned applications. With the distances involved, terrestrial data centers may respond too slowly for mission-critical information or for satisfying entertainment. It would be very advantageous to bring MRAM storage devices along with the vehicle, platform, or the like. This would essentially eliminate the latency due to the need to communicate with terrestrial data centers.

[0008] Computing and storage devices must be kept within temperature limits of their internal circuits to optimize performance. However, heat shields, cooling, or heating all add mass to the mission. Added mass equates to greatly increased launch costs. Temperatures can vary widely depending upon the usage of the storage device. This is particularly true in space applications, where there are enormous temperature differences between, for example, shaded areas of a vehicle and sunlit areas of the vehicle.

[0009] Thus what is needed is a temperature robust data storage system that does not add excessive mass to the vehicle. What is needed is a reliable memory system that can function reliably across a broad temperature range.

SUMMARY OF THE INVENTION

[0010] Embodiments of the present invention implement a system for a temperature robust nonvolatile memory for broad temperature range applications. Embodiments of the present invention implement a temperature robust MRAM data storage system that does not add excessive mass to the memory system. Embodiments of the present invention provide a reliable MRAM system that can function reliably across a broad temperature range, and is useful for automotive, aeronautics, military, space exploration, and other such systems that require operation across a broad temperature range.

[0011] In one embodiment, the present invention is implemented as a system for a temperature robust nonvolatile memory for broad temperature range applications. The system includes a memory organized into an addressable memory range and comprising a plurality of memory arrays comprising memory cells wherein each memory array is configured for operation over a different temperature range, and a buffer for receiving data words and associated

addresses for writing into the memory. A temperature sensor is used for sensing a current temperature of operation of the memory. A write controller is coupled to the buffer, the temperature sensor and the memory, the write controller is operable to perform write operations that include accessing temperature values from the temperature sensor, selecting a selected memory array of the plurality of memory arrays that is configured for operation at a current temperature value, and writing the data words, at the associated addresses, to the selected memory array.

[0012] In this manner, the system includes a plurality of MRAM memory arrays. Each of the memory arrays is tuned to be optimized at a different temperature range (e.g., low temperature, medium temperature, high temperature, etc.). The system further includes a temperature sensor coupled to the controller, which allows targeted read/write access to a particular one of the memory arrays based on a current temperature reading. Importantly, the system does not need to be insulated to reduce temperature variations which would typically occur in space applications and in some mobile applications.

[0013] Accordingly, an advantage of the present invention is to reduce the amount of environmental control (HVAC) and insulation that needs to be moved around (e.g. launched on the space vehicle) as opposed to being specifically disposed around the system. This is due to the fact that the system is designed to reliably operate across a broad range of temperatures. The solution of the present invention, as described above, is to use a plurality of temperature optimized MRAM memory arrays. Each of the memory arrays is tuned to be optimized at a different temperature range (e.g., low temperature, medium temperature, high temperature, etc.). Different examples as to what could cause temperatures to change would be, for example, if the system is on a space vehicle and something blocks out the sun (e.g., a solar panel, etc.), or if the space vehicle is in the shade (e.g., on the nighttime side of Earth) and it passes into sunlight. Another example would be a vehicle housed in a garage, and that same vehicle later parked during the daytime in the desert (e.g. Phoenix). Other examples include military, aeronautic, automotive and any other application that requires operation across a broad temperature range.

[0014] In one embodiment, the memory cells of the plurality of memory arrays comprise magnetic memory cells.

[0015] In one embodiment, the magnetic memory cells comprise Magnetic Tunnel Junction type magnetic memory cells.

[0016] In one embodiment, a memory table is associated with the memory, wherein the memory table is operable to store an address map for indicating which memory array of the plurality of memory arrays comprises a data word associated with a given address within the addressable memory range.

[0017] In one embodiment, the present invention is implemented as a read controller coupled to the buffer, the temperature sensor and the memory, the read controller operable to perform a read operation. The read operation includes accessing a read address from the buffer wherein the read address is associated with the read operation, reading contents of the memory table associated with the read address to determine a particular memory array of the plurality of memory arrays containing data associated with the read address, and reading the particular memory array, at the read address, to obtain a data word associated with the read address.

[0018] In one embodiment, the plurality of memory arrays includes a first memory array comprising a plurality of first memory cells that are fabricated to operate over a first temperature range, a second memory array comprising a plurality of second memory cells that are fabricated to operate over a second temperature range, wherein the second temperature range is higher than the first temperature range, and a third memory array comprising a plurality of third memory cells that are fabricated to operate over a third temperature range, wherein the third temperature range is higher than the second temperature range and wherein the second temperature range is higher than the first temperature range and wherein further a high temperature of the first temperature range and a low temperature of the second temperature range overlap and wherein further a high temperature of the second temperature range and a low temperature of the third temperature range overlap.

[0019] In one embodiment, a management controller is coupled to the memory and the temperature sensor, the management controller for performing a copy-over procedure. The procedure includes reading a current temperature value from the temperature sensor, based on the current temperature value, determining that the memory has undergone a transition from operating within a first temperature range to operating within a second temperature range, selecting a first memory array associated with the first temperature range and selecting a second memory array associated with the second temperature range, and copying data from the first memory array over to the second memory array responsive to the transition.

[0020] In one embodiment, a management controller is coupled to the memory and the temperature sensor, the management controller for performing a copy-over procedure. The procedure includes reading a current temperature value from the temperature sensor, based on the current temperature value, determining that the memory has undergone a transition from operating within a first temperature range to operating within a second temperature range, selecting a first memory array associated with the first temperature range and selecting a second memory array associated with the second temperature range. The procedure further includes copying data from the first memory array over to the second memory array responsive to the transition, and updating the address map of the memory table to indicate that the data copied from the copying is addressable using the second memory array.

[0021] In one embodiment, the present invention is implemented as method of writing data to a memory system, the method including receiving a data word and an associated address for writing into the memory system, wherein the memory system is organized into an addressable memory range and comprises a plurality of memory arrays comprising memory cells wherein each memory array of the plurality of memory arrays is configured for operation over a different temperature range, accessing a current temperature value from a temperature sensor, selecting a selected memory array of the plurality of memory arrays that is configured for operation at the current temperature value, and writing the data word, at the associated address, to the selected memory array.

[0022] In one embodiment, the present invention is implemented as a method of storing data in a memory system. The method includes maintaining an address map of data stored in a memory system, wherein the memory system is organized into an addressable memory range and comprising a plurality of memory arrays comprising memory cells wherein each memory array of the plurality of memory arrays is configured for operation over a different temperature range and wherein further the memory system is configured to operate over a plurality of temperature ranges. The address map indicates which memory array of the plurality of memory arrays comprises a data word associated with a given address. The method further includes reading a current temperature value from a temperature sensor, based on the current temperature value, determining that the memory system has undergone a transition from operating within a first temperature range of the plurality of temperature ranges to operating within a second temperature range of the plurality of temperature ranges, selecting a first memory array associated with the first temperature range and selecting a second memory array associated with the second temperature range, copying data from the first memory array over to the second memory array responsive to the transition, and updating the memory map based on the copying.

[0023] The foregoing is a summary and thus contains, by necessity, simplifications, generalizations and omissions of detail; consequently, those skilled in the art will appreciate that the summary is illustrative only and is not intended to be in any way limiting. Other aspects, inventive features, and advantages of the present invention, as defined solely by the claims, will become apparent in the non-limiting detailed description set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements.

[0025] FIG. **1** shows two exemplary applications of a memory array system in accordance with one embodiment of the present invention.

[0026] FIG. **2** shows a memory organized into an addressable memory range and comprising a plurality of discrete memory arrays comprising memory cells wherein each memory array is configured for operation over a different temperature range in accordance with one embodiment of the present invention.

[0027] FIG. **3** depicts a system for a temperature robust nonvolatile memory for broad temperature range applications in accordance with one embodiment of the present invention.

[0028] FIG. **4** shows a diagram showing a temperature range of operation for a plurality of memory arrays in accordance with one embodiment of the present invention.

[0029] FIG. **5**A shows a flowchart of the steps of an exemplary data writing process in accordance with one embodiment of the present invention.

[0030] FIG. **5**B shows a flowchart of the steps of a reading process in accordance with one embodiment of the present invention.

[0031] FIG. **6**A shows a flowchart of the steps of an exemplary data writing process in accordance with one alternative embodiment of the present invention.

[0032] FIG. **6**B shows a flowchart of the steps of a reading process in accordance with one alternative embodiment of the present invention.

[0033] FIG. **7** shows a flowchart of the steps of a controlling process in accordance with one embodiment of the present invention.

[0034] FIG. **8** shows a flowchart of the steps of a copy over process in accordance with one embodiment of the present invention responsive to a detected temperature change of the memory system.

DETAILED DESCRIPTION

[0035] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of embodiments of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the embodiments of the present invention.

A System for a Wide Temperature Range Nonvolatile Memory

[0036] Embodiments of the present invention implement a system for a temperature robust nonvolatile memory for broad temperature range applications. Embodiments of the present invention implement a temperature robust MRAM data storage system that does not add excessive mass to the memory system. Embodiments of the present invention provide a reliable MRAM system that can function reliably across a broad temperature range, and is useful for automotive, aeronautics, military, space exploration, and other such systems that require operation across a broad temperature range. Other such systems can include extreme temperatures encountered in drilling or in geological sensing applications.

[0037] In one embodiment, the present invention is implemented as a system for a temperature robust nonvolatile memory. The system includes a memory organized into an addressable memory range and comprising a plurality of memory arrays comprising memory cells wherein each memory array is configured for operation over a different temperature range, and a buffer for receiving a data word and an associated address for writing into the memory. A temperature sensor is used for sensing a current temperature of operation of the memory. A write controller is coupled to the buffer, the temperature sensor and the memory, the write controller operable to perform a write operation that includes accessing a temperature value from the temperature sensor, selecting a selected memory array of the plurality of memory arrays that is configured for operation at the temperature value, and writing the data word, at the associated address, to the selected memory array.

[0038] In this manner, the system includes a plurality of MRAM memory arrays. Each of the memory arrays is tuned to be optimized at a different temperature (e.g., low temperature, medium temperature, high temperature, etc.). The system further includes a temperature sensor coupled to the controller, which allows targeted read write access to a particular one of the memory arrays based on a current temperature reading. Importantly, the system does not need to be insulated to reduce temperature variations which would typically occur in space applications and some mobile applications, for example.

[0039] FIG. **1** shows two exemplary applications of a memory array system in accordance with one embodiment of the present invention. FIG. **1** shows an image **102** depicting the interior of a space vehicle for taking humans into space (e.g., space tourism, etc.) and an image **104** depicting a human a vehicle in outer space (e.g., space tourism, recreation, etc.). Of course, these are merely exemplary uses.

[0040] Accordingly, one advantage of the present invention is to reduce the amount of environmental control (HVAC) and insulation that needs to be moved around (e.g. launched on the space vehicle). This is due to the fact that the system is designed to reliably operate across a broad range of temperatures. The solution of the present invention, as described above, is to use a plurality of temperature optimized MRAM memory arrays. Each of the memory arrays is tuned to be optimized at a different temperature (e.g., low temperature, medium temperature, high temperature, etc.). Different examples as to what could cause temperatures to change would be, for example, if the system is on a space vehicle and something blocks out the sun (e.g., a solar panel, etc.), or if the space vehicle is in the shade (e.g., on the nighttime side of Earth) and it passes into sunlight. Another example would be a vehicle housed in a garage, and that same vehicle later parked during the daytime in the desert (e.g. Phoenix).

[0041] FIG. **2** shows a memory organized into an addressable memory range and comprising a plurality of memory arrays comprising memory cells wherein each memory array is configured for operation over a different temperature range in accordance with one embodiment of the present invention. In the FIG. **2** embodiment, three memory arrays **202-206** are shown. Memory array **202** is fabricated using semiconductor processes that are optimized for low temperatures. This means that reading and writing occurs most efficiently at low temperature. Memory array **204** is similarly fabricated such that it is optimized for medium temperatures. Memory array **206** is fabricated such that it is optimized for high temperatures (e.g., most efficient operation at high temperature). Thus, each memory array **202-206** is configured for operation over a different temperature range. When all three arrays **202-206** are integrated into a single memory, its operability is across the low to high temperature ranges.

[0042] FIG. **3** depicts a system **300** for a temperature robust nonvolatile memory broad temperature range applications in accordance with one embodiment of the present invention. The system **300** includes a memory **302** organized into an addressable memory range and comprising a plurality of memory arrays **304** comprising memory cells. In one embodiment, each of the memory arrays **304** are configured for operation over a different temperature range, Δ_0 Δ_1, . . . , $\Delta_{(n-1)}$.

[0043] A buffer **306** is shown for receiving data and addresses from an input output port **308**. Such data typically comprises data words and associated addresses and commands for writing into the memory **302**. A temperature sensor **310** is used for sensing a current temperature of operation of the memory **300**. A controller **314** is coupled to the buffer **302**, the temperature sensor **310** and the memory **302**.

[0044] In one embodiment, the controller **314** is operable to perform read and write operations that includes accessing a temperature value from the temperature sensor **310**, selecting a selected memory array of the plurality of memory arrays **304** that is configured for operation at the temperature value, and writing the data word, at the associated address, to the selected one of the memory arrays **304**.

[0045] It is appreciated that when the data or ECC (error correction coding) encoded data and parity come into the buffer **306**, what also comes is the address to which the data is to be written and commands for the controller (e.g. write data, read data, synchronize, etc.). In the FIG. **3** embodiment, the data addresses and commands come in from the left through the port **308** to the buffer **306** and then on to controller **314**, where the controller has to decide based upon the commands what to do with the data. A typical command would be for example, to read or write data, and the controller has to decide what memory array with which to do the reading or the writing based on the currently reported temperature.

[0046] In one embodiment, the memory cells of the plurality of memory arrays comprise magnetic memory cells. In one embodiment, the magnetic memory cells comprise Magnetic Tunnel Junction type magnetic memory cells. Magnetic tunnel junction memory cells are popular for use in storage systems since they are nonvolatile.

[0047] In one embodiment, a memory table **340** is associated with the memory **302**. The memory table **340** is operable to store one or more address maps for indicating which memory array of the plurality of memory arrays **304** comprises a data word associated with a given address within the addressable memory range.

[0048] It should be noted that in one embodiment, memory table **340** would be straightforward since it would only point to one of the memory arrays based upon the current temperature. If the system **300** has experienced a stable temperature over a long period, the system is only using one memory array. The memory table indicates which memory array the system needs to copy over to (e.g., synchronize) when the temperature is changing. It should be noted that in other embodiments the memory table **340** could be much more complicated if the data is distributed all across the memory arrays. The level of complexity of the memory table **340** thus varies with multiple use case scenarios.

[0049] In one embodiment, the system **300** of the present invention includes a read controller **322** coupled to the buffer, the temperature sensor **310** and the memory **302**. The read controller **322** is operable to perform read operations for system **300**. The read operations include accessing a read address from the buffer **306**. The read address is associated with the read operation, reading contents of the memory table **340** associated with the read address to determine a particular memory array of the plurality of memory arrays **304** containing data associated with the read address, and

reading the particular memory array, at the read address, to obtain a data word associated with the read address.

[0050] In one embodiment, the system **300** of the present invention includes a write controller **320** coupled to the buffer **306**. The write controller **320** is also coupled to the temperature sensor **310** and the memory **302**. The write controller **320** is operable to perform write operations. The write operations include accessing a write address from the buffer **306**. The write address is associated with the write operation, reading contents of the memory table **340** associated with the write address to determine a particular memory array of the plurality of memory arrays **304** to write the data word, and to write the particular memory array, at the write address, the data word associated with the write address.

[0051] In one embodiment, the controller **314** includes a management controller **324**. The management controller **324** is the part of the controller **314** operable for managing operations of the controller **314** that includes accessing a temperature value from the temperature sensor **310**, selecting a selected memory array of the plurality of memory arrays **304** that is configured for operation at the temperature value, and commanding the reading and writing of data words, at the associated addresses, to the selected ones of the memory arrays **304**.

[0052] In one embodiment, the power monitor **312** functions by maintaining local power (e.g., such as a capacitor) so that if a write is in progress, the capacitor can provide enough backup power to ensure the write is completed. For example, in one embodiment, if externally provided power begins to drop, the power monitor **312** can take steps to preserve data within a few milliseconds. One example is where the power monitor indicates that data needs to be flushed from volatile memory to nonvolatile memory. The power monitor **312** provides a source of local power to ensure synchronizations are not corrupted.

[0053] FIG. **4** shows a diagram **400** showing a plurality of operating temperature ranges of operation for a plurality of memory arrays in accordance with one embodiment of the present invention. As shown in FIG. **4**, five exemplary memory arrays **402-410** are shown. The five memory arrays **402-410** are optimized to function along the broad temperature range **440**, with memory array **402** optimized for the lowest temperature range, memory array **404** optimized for the next lowest temperature range, and so on until reaching memory array **410** which is optimized for the highest temperature range.

[0054] It should be noted that each of the memory arrays **402-410** are fabricated to allow an amount of overlap in the temperature range between itself and its neighbor. This depicted as the overlaps **450-456** in adjacent temperature ranges.

[0055] In one embodiment, where the system is currently at a low temperature and reading and writing are proceeding to a low temperature memory array (e.g., memory array **402**), as the temperature begins to rise, eventually the system is going to have to transition to reading and writing to the next higher temperature memory array (e.g., memory array **404**). Embodiments of the present invention include a process to automatically synchronize data between the memory arrays during a temperature change. An objective of the invention is to be able to operate across a comparatively broad range of temperatures. As depicted in FIG. **4**, there is some overlap in the temperature ranges in at which neighboring memory arrays are functional. For example when temperature is rising, and is threatening to rise past the overlap area, the data from the low temperature memory array (e.g., memory array **402**) is transferred to the next higher temperature memory array (e.g., memory array **404**). This ensures data is not lost as temperature continues to rise. The same is true when the temperature is falling and thus a range transition occurs.

[0056] This process is referred to as synchronization between the low temperature memory array and the next higher temperature memory array or vice versa on a falling temperature, e.g., the process is reversed when temperature is declining. For example, when temperature dictates that reading and writing occur in a high temperature memory array (e.g., memory array **410**), when the temperature begins to decline, and reaches the overlap area (e.g., overlap area **456**), the data from the high temperature memory array is transferred to the next lower temperature memory array (e.g., synchronized). In one embodiment, ECC (error correction coding) helps with the synchronization both with increasing temperatures and decreasing temperatures.

[0057] In one embodiment, temperature optimized overlap synchronization is more critical when temperatures are rising. In one embodiment, at low temperatures it is typically too difficult and error prone to write to the higher temperature memory arrays. In one embodiment, attempting to do so leads to an unacceptable error rate.

[0058] It should be noted that during synchronization, the controller has to make decisions as to whether a complete copy of the data is synchronized from one memory array to the next. Depending upon different use case scenarios, in cases where the data that needs to be transferred is the code itself that runs the system, that data would need to be transferred in its entirety. Another use case scenario is a rolling log. This would be a case where after a certain amount of time the data that is logged is no longer useful to the system, and in this case there would be no need to transfer the stale data. For example, in a spaceflight use case scenario, space tourists go into space and they want to have streaming video and audio and they also want to capture their own video and audio of their journey. The resulting footage would be completely copied over during synchronization to ensure it is not lost to the tourists.

[0059] In one embodiment, the system is configured to perform extreme error recovery by reading the data from more than one array and voting on a valid data value (e.g., or apply some other ECC method).

[0060] In one embodiment, the system is configured for fast writing at high temperatures. For example, at high temperatures the low-temperature array is written to first (e.g., it writes faster). Then, based on time, and not temperature, the data is written from the low-temp array to higher and higher temp arrays until the correct temperature array is reached. The point of such a configuration is that lower delta MTJs write faster but they do not hold the data long enough.

[0061] FIG. **5**A shows a flowchart of the steps of an exemplary data writing process **500** in accordance with one embodiment of the present invention. FIG. **5**A begins in step **502**, where data and error correction code are received by the system (e.g., by the buffer **306**). In step **504**, a temperature sensor provides temperature information to a controller (e.g., controller **314**) of the current temperature of the memory system and this information is used to determine

which bank (e.g., memory array) is to be used for writing the data. As described above this depends on what the current temperature is. And subsequently in step **508**, the data is written to the appropriate bank.

[0062] FIG. **5**B shows a flowchart of the steps of a reading process **520** in accordance with one embodiment of the present invention. In step **524**, a temperature sensor provides temperature information to a controller (e.g., controller **314**) to determine which bank (e.g., memory array) is to be read from. As described above this depends on what the current temperature is. And in step **526**, the data is read from the appropriate bank and into the buffer **306**. Subsequently, in step **528**, the data and error correction code is output through the port **308** (e.g., and goes to an ECC decoding engine).

[0063] FIG. **6**A shows a flowchart of the steps of an exemplary data writing process **600** in accordance with one alternative embodiment of the present invention. FIG. **6**A begins in step **602**, where data and error correction code are received by the system (e.g., by the buffer **306**). In step **604**, a temperature sensor provides temperature information to a controller (e.g., controller **314**) of the current temperature of the memory system and this information is used to determine which bank (e.g., memory array) is to be used for writing the data. As described above this depends on what the current temperature is. And subsequently in step **608**, the data is written to the appropriate bank. In step **610**, the memory map table is updated to include the address and bank of the data write.

[0064] FIG. **6**B shows a flowchart of the steps of a reading process **620** in accordance with one alternative embodiment of the present invention. In step **624**, a memory map table is accessed to obtain and provide addresses to a controller (e.g., controller **314**) to determine the address and which bank (e.g., memory array) is to be read from. As described above this depends on what the current temperature is. And in step **626**, the data is read from the appropriate bank and into the buffer **306**. Subsequently, in step **628**, the data and error correction code is output through the port **308**.

[0065] FIG. **7** shows a flowchart of the steps of a controlling process **700** in accordance with one embodiment of the present invention. FIG. **7** shows the exemplary steps of a state machine executed by a controller (e.g., controller **314**). Process **700** starts at step **702** when a state machine commences operation. In step **704**, a temperature sensor provides temperature information to a controller. In step **706** the controller compares the temperature information against previously received temperature information to determine whether there is a change in temperature. If there is no change in temperature, process **700** remains in step **706**. If there is a change in temperature, process **700** proceeds to step **708** were it reads data from the most recent selected bank (e.g., memory array). This selected memory array is typically the last memory array which was read or written to at the previous temperature. In step **710**, data is written to the newly selected best memory array based upon the new temperature. Subsequently process **700** proceeds back to step **706** where temperature readings are again monitored from the temperature sensor.

[0066] FIG. **8** shows a flowchart of the steps of a copy over process **800** in accordance with one embodiment of the present invention. Process **800** begins in step **802**, where a current temperature value is read from a temperature sensor. In step **804**, based on the current temperature, process **800** determines whether the system has undergone a transition from operating within a first temperature range (e.g., low temperature) to operating within a second temperature range (e.g., medium temperature). In step **806**, a first memory array associated with the first temperature range is selected. A second memory array associated with a second temperature range is also selected. In step **808**, data from the first memory array is copied over to the second memory array in response to the transition. In step **810**, the memory map table is updated in accordance with the copy over.

[0067] In this manner, embodiments of the present invention implement a system for a temperature robust nonvolatile memory for operation across broad temperature ranges. Embodiments of the present invention implement a temperature robust MRAM data storage system that does not add excessive mass to the vehicle. Embodiments of the present invention provides a reliable MRAM system that can function reliably across a broad temperature range.

[0068] The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

1. A system comprising:

a memory organized into an addressable memory range and comprising a plurality of memory arrays comprising memory cells wherein each memory array is configured for operation over a different temperature range;

a buffer for receiving a data word and an associated address for writing into said memory;

a temperature sensor for sensing a current temperature of operation of said memory;

a write controller coupled to said buffer, said temperature sensor and said memory, said write controller operable to perform a write operation comprising:

accessing a temperature value from said temperature sensor;

selecting a selected memory array of said plurality of memory arrays that is configured for operation at said temperature value; and

writing said data word, at said associated address, to said selected memory array; and

a memory table associated with said memory, wherein said memory table is operable to store an address map for indicating which memory array of said plurality of memory arrays comprises a data word associated with a given address within said addressable memory range.

2. A system as described in claim **1** wherein said memory cells of said plurality of memory arrays comprise magnetic memory cells.

3. A system as described in claim **2** wherein said magnetic memory cells comprise Magnetic Tunnel Junction type magnetic memory cells.

4. (canceled)

5. A system as described in claim **1** further comprising a read controller coupled to said buffer, said temperature

sensor and said memory, said read controller operable to perform a read operation comprising:

accessing a read address from said buffer wherein said read address is associated with said read operation;

reading contents of said memory table associated with said read address to determine a particular memory array of said plurality of memory arrays containing data associated with said read address; and

reading said particular memory array, at said read address, to obtain a data word associated with said read address.

6. A system as described in claim **1** wherein said plurality of memory arrays comprises:

a first memory array comprising a plurality of first memory cells that are fabricated to operate over a first temperature range;

a second memory array comprising a plurality of second memory cells that are fabricated to operate over a second temperature range, wherein said second temperature range is higher than said first temperature range; and

a third memory array comprising a plurality of third memory cells that are fabricated to operate over a third temperature range, wherein said third temperature range is higher than said second temperature range and wherein said second temperature range is higher than said first temperature range and wherein further a high temperature of said first temperature range and a low temperature of said second temperature range overlap and wherein further a high temperature of said second temperature range and a low temperature of said third temperature range overlap.

7. A system as described in claim **1** further comprising a management controller coupled to said memory and said temperature sensor, said management controller for performing a copy-over procedure comprising:

reading a current temperature value from said temperature sensor;

based on said current temperature value, determining that said memory has undergone a transition from operating within a first temperature range to operating within a second temperature range;

selecting a first memory array associated with said first temperature range and selecting a second memory array associated with said second temperature range; and

copying data from said first memory array over to said second memory array responsive to said transition.

8. A system as described in claim **4** further comprising a management controller coupled to said memory and said temperature sensor, said management controller for performing a copy-over procedure comprising:

reading a current temperature value from said temperature sensor;

based on said current temperature value, determining that said memory has undergone a transition from operating within a first temperature range to operating within a second temperature range;

selecting a first memory array associated with said first temperature range and selecting a second memory array associated with said second temperature range;

copying data from said first memory array over to said second memory array responsive to said transition; and

updating said address map of said memory table to indicate that said data copied from said copying is addressable using said second memory array.

9. A method of writing data to a memory system, said method comprising:

receiving a data word and an associated address for writing into said memory system, wherein said memory system is organized into an addressable memory range and comprises a plurality of memory arrays comprising memory cells wherein each memory array of said plurality of memory arrays is configured for operation over a different temperature range;

accessing a current temperature value from a temperature sensor;

selecting a selected memory array of said plurality of memory arrays that is configured for operation at said current temperature value;

writing said data word, at said associated address, to said selected memory array;

maintaining an address map within a memory table wherein said address map indicates which memory array of said plurality of memory arrays comprises a data word associated with a given address of said addressable memory range; and

responsive to said writing, updating said address map to indicate that said associated address is associated with said selected memory array.

10. A method as described in claim **9** wherein said memory cells of said plurality of memory arrays comprise magnetic memory cells.

11. A system as described in claim **10** wherein said magnetic memory cells comprise Magnetic Tunnel Junction type magnetic memory cells.

12. (canceled)

13. A method as described in claim **9** further comprising performing a read operation, said read operation comprising:

accessing a read address associated with said read operation;

reading contents of said memory table associated with said read address to determine a particular memory array of said plurality of memory arrays containing data associated with said read address; and

reading said particular memory array, at said read address, to obtain a data word associated with said read address.

14. A method as described in claim **9** wherein said plurality of memory arrays comprises:

a first memory array comprising a plurality of first memory cells that are fabricated to operate over a first temperature range;

a second memory array comprising a plurality of second memory cells that are fabricated to operate over a second temperature range, wherein said second temperature range is higher than said first temperature range; and

a third memory array comprising a plurality of third memory cells that are fabricated to operate over a third temperature range, wherein said third temperature range is higher than said second temperature range and wherein said second temperature range is higher than said first temperature range and wherein further a high temperature of said first temperature range and a low temperature of said second temperature range overlap and wherein further a high temperature of said second temperature range and a low temperature of said third temperature range overlap.

15. A method as described in claim **9** further comprising performing a copy-over procedure comprising:

reading a current temperature value from said temperature sensor;

based on said current temperature, determining that said memory has undergone a transition from operating within a first temperature range to operating within a second temperature range;

selecting a first memory array associated with said first temperature range and selecting a second memory array associated with said second temperature range; and

copying data from said first memory array over to said second memory array responsive to said transition.

16. A method as described in claim **12** further comprising performing a copy-over procedure comprising:

reading a current temperature value from said temperature sensor;

based on said current temperature, determining that said memory has undergone a transition from operating within a first temperature range to operating within a second temperature range;

selecting a first memory array associated with said first temperature range and selecting a second memory array associated with said second temperature range;

copying data from said first memory array over to said second memory array responsive to said transition; and

updating said address map to indicate that data copied from said copying is addressable by said second memory array.

17. A method of storing data in a memory system, said method comprising:

maintaining an address map of data stored in a memory system, wherein said memory system is organized into an addressable memory range and comprising a plurality of memory arrays comprising memory cells wherein each memory array of said plurality of memory arrays is configured for operation over a different temperature range and wherein further said memory system is configured to operate over a plurality of temperature ranges, and wherein said address map indicates which memory array of said plurality of memory arrays comprises a data word associated with a given address;

reading a current temperature value from a temperature sensor;

based on said current temperature value, determining that said memory system has undergone a transition from operating within a first temperature range of said plurality of temperature ranges to operating within a second temperature range of said plurality of temperature ranges;

selecting a first memory array associated with said first temperature range and selecting a second memory array associated with said second temperature range;

copying data from said first memory array over to said second memory array responsive to said transition; and

updating said memory map based on said copying.

18. A method as described in claim **17** wherein said memory cells of said plurality of memory arrays comprise magnetic memory cells.

19. A system as described in claim **18** wherein said magnetic memory cells comprise Magnetic Tunnel Junction type magnetic memory cells.

20. A method as described in claim **17** further comprising performing a read operation, said read operation comprising:

accessing a read address associated with said read operation;

reading contents of said address map associated with said read address to determine a particular memory array of said plurality of memory arrays containing data associated with said read address; and

reading said particular memory array, at said read address, to obtain a data word associated with said read address.

21. A method as described in claim **17** wherein said plurality of memory arrays comprises:

a first memory array comprising a plurality of first memory cells that are fabricated to operate over a first temperature range;

a second memory array comprising a plurality of second memory cells that are fabricated to operate over a second temperature range, wherein said second temperature range is higher than said first temperature range; and

a third memory array comprising a plurality of third memory cells that are fabricated to operate over a third temperature range, wherein said third temperature range is higher than said second temperature range and wherein said second temperature range is higher than said first temperature range and wherein further a high temperature of said first temperature range and a low temperature of said second temperature range overlap and wherein further a high temperature of said second temperature range and a low temperature of said third temperature range overlap.

22. A method as described in claim **17** further comprising performing a write operation, said write operation comprising:

accessing said temperature sensor to obtain a current temperature value;

receiving a data word and an associated address for writing into said memory system;

selecting a selected memory array of said plurality of memory arrays that is configured for operation at said current temperature value;

writing said data word, at said associated address, to said selected memory array; and

updating said address map responsive to said writing.

23. A method as described in claim **17**, further comprising performing extreme error recovery by reading the data from a plurality of memory arrays and voting on a valid data value.

24. A method as described in claim **17**, further comprising performing extreme error recovery by reading the data from a plurality of memory arrays and applying error correction coding to obtain a valid data.

25. A method as described in claim **17**, further comprising, writing to the low-temperature array is written to first at high temperature, and based on a time value, writing from the low-temp array to a higher temperature array until a correct temperature array is reached.

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